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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/918,023	07/30/2001	Paul J. Mantey	10016249-1	1038

7590 07/30/2004

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EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/918,023	MANTEY ET AL.	
	Examiner	Art Unit	
	Nimesh G Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5,6 and 11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-6 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 5-6 are objected to because of the following informalities: It appears the claims are dependent on claim 134 because the strikethrough line corresponds with the parallel line in the number four. Applicant can put double brackets around the number so that it can be clear the claims depend on claim 13 and not claim 134. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 5-6, and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, in view of Smiley('297).

5. Regarding claim 11, admitted prior art discloses a system comprising: a plurality of interconnected circuit boards(Figure 1, 100 and 102), at least two of the plurality of interconnected circuit boards embodying at least one FPGA(Figure 1, 104) coupled to a configuration EEPROM(Figure 1, 108) of the type capable of being programmed over a serial

bus; wherein at least one EEPROM of a circuit board of the plurality of circuit boards is coupled to a first serial bus(Figure 1, 108), and at least one EEPROM of a circuit board of the plurality of circuit boards is coupled to a second serial bus(Figure 1, 126).

The admitted prior art does not disclose a common configuration point apparatus coupled to the first serial bus and to the second serial bus, the common configuration point apparatus further comprising: selection apparatus for selecting a particular bus of the first and second serial busses; and coupling apparatus for coupling configuration signals to the particular bus of the plurality of serial busses. The admitted prior also does not disclose at least one EEPROM of the first serial bus and at least one EEPROM of the second serial bus containing board identification information.

However, Smiley discloses a common configuration point apparatus(Figure 1, ISPM), the common configuration point apparatus further comprising: selection apparatus for selecting a particular bus of the first and second serial busses; coupling apparatus for coupling configuration signals to the particular bus of the plurality of serial busses, and at least one EEPROM of the first serial bus and at least one EEPROM of the second serial bus containing board identification information(Column 5, Lines 54-60; The address strap field can be used to select any serial bus to be programmed). Therefore, it would have been obvious to combine admitted prior art with the teachings of Smiley because it would save manpower and time in connecting and disconnecting the configuration system(Column 1, Lines 19-23).

6. Regarding claim 12, admitted prior art discloses the first serial bus and the second serial bus are of the JTAG type(Paragraph 11).

7. Regarding claim 13, the admitted prior art discloses a method of in-system programming of EEPROMs, the EEPROMs coupled to provide configuration code to programmable logic devices(Paragraph 11), each EEPROM being located on a particular circuit board of a plurality

of circuit boards of a system and wherein not all EEPROMs are located on the same circuit board(Figure 1), comprising: providing a plurality of board-specific serial busses of the Joint Test Action Group (JTAG) type(Figure 1, 111 & 126), each board-specific serial bus coupling to EEPROMs of a particular circuit board(Figure 1); erasing at least one EEPROM coupled to the particular board-specific serial bus; writing programmable logic device configuration code through the selected board-specific serial bus to the at least one EEPROM(Paragraph 12); wherein the programmable logic device configuration code comprises configuration code for at least one FPGA(Paragraph 12); and verifying compatibility of the configuration code is with a circuit board embodying at least one EEPROM coupled to the board-specify serial bus(Paragraphs 12-13; The XILINX datasheet for the DS026, as admitted by the applicant, discloses a security bit that is used to allow the reading, i.e. verifying, the configuration code(Page 5, Design Security)).

The admitted prior art does not disclose coupling the plurality of board-specific serial busses to a common configuration point having selection apparatus; coupling the common configuration point to configuration apparatus capable of interacting with at least one serial bus to program EEPROMS; setting the selection apparatus to select a particular board-specific serial bus of the plurality of board-specific serial busses; and reading board identification information through the board-specific serial bus to the configuration apparatus.

However Smiley discloses coupling the plurality of board-specific serial busses to a common configuration point having selection apparatus(Figure 1, ISPM); coupling the common configuration point to configuration apparatus capable of interacting with at least one serial bus to program EEPROMS; setting the selection apparatus to select a particular board-specific serial bus of the plurality of board-specific serial busses; and reading board identification information through the board-specific serial bus to the configuration apparatus(Column 5, Lines

54-60; The address strap field can be used to select any serial bus to be programmed). Therefore, it would have been obvious to combine admitted prior art with the teachings of Smiley because it would save manpower and time in connecting and disconnecting the configuration system(Column 1, Lines 19-23).

8. Regarding claim 5, admitted prior art discloses at least one EEPROM device is collocated on the same die as at least one FPGA(Figure 1).

9. Regarding claim 6, admitted prior art discloses the step of loading at least one of the programmable logic devices with configuration code from at least one of the EEPROMs(Paragraph 12).

10. Regarding claim 14, Smiley discloses a method, further comprising the step of selecting a configuration code from a file containing a plurality of configuration codes according to the board identification information(Column 2, Lines 30-36).

Response to Arguments

11. Applicant's arguments with respect to claims 5-6 and 11-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 703-305-7583. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP NP
July 14, 2004

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100